PCT

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H04L 12/12, G06F 1/26

A1

(11) International Publication Number: WO 96/13106

(43) International Publication Date: 2 May 1996 (02.05.96)

(21) International Application Number: PCT/US95/12128

(22) International Filing Date: 25 September 1995 (25.09.95)

(30) Priority Data:
08/326,691 20 October 1994 (20.10.94) US

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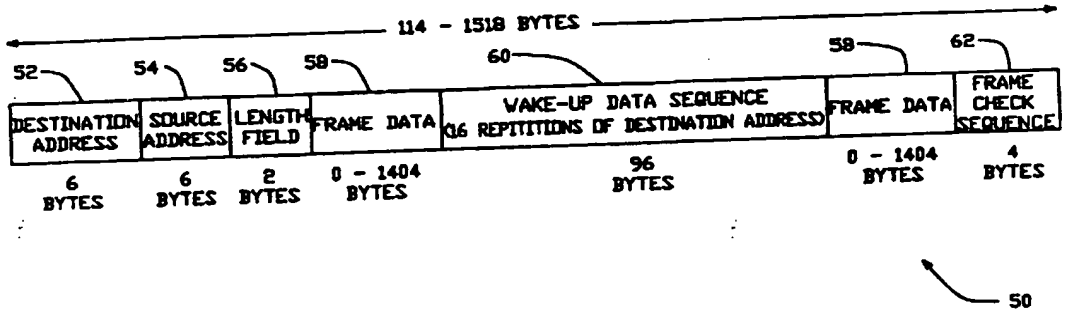
(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: SYSTEM AND METHOD FOR REMOTE WAKE-UP



(57) Abstract

A system and method for remotely waking up a device (10) connected to a local area network (LAN) is disclosed. A special data packet (50) is disclosed wherein the destination address of the packet is embedded at least 16 consecutive times within the data field (60) of the packet. When this particular type of packet is transmitted on the LAN, it is first decoded by the I/O subsystem (12) of the device to determine whether or not it is a remote wake-up packet. After determining that the packet received is a remote wake-up packet, a wake-up enable line (13) is activated thereby taking the system out of its low power mode, for providing further processing of future received packets.

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SYSTEM AND METHOD FOR REMOTE WAKE-UP

BACKGROUND OF INVENTION

Field of the Invention

This invention relates generally to local area networks (LAN's), and more particularly to the remote wake-up of components connected to a local area network.

Description of the Related Art

Communication between multiple users across vast distances via a network has become almost a necessity in today's global marketplace. A Local Area Network (LAN) is a specific type of network which can support peer-to-peer communication over distances of tens of meters to several kilometers. A specific type of LAN is the ethernet, where information from multiple users travels through the network by use of a system bus in the form of discreet packets containing a number of pieces of information. A typical information packet contains a series of fields: a Destination Address Field; a Source Address Field; a Length Field; a Data Field where the user information is present and, in some cases, an error checking field.

Presently, there is a trend, due to the increasing use of lap top and other portable computers which operate on battery power for manufacturers to

develop systems that have power conservation features or that can operate in a low power mode. Due to the increasing consumer demand for low power operation capability, the ability to wake-up a remote device in the SLEEP (low power) mode without the use of the Central Processing Unit (CPU) or other Power Management circuitry which requires a lot of power and decreases battery life is becoming increasingly important to manufacturers. For a device that is in a low power mode, there is no simple and efficient way to determine where information packets that are received by the device through the network should be sent. In present systems, the CPU would have to be activated to process the incoming information to see if the entire device should be activated. This requires the use of a lot of extra hardware which uses a lot of energy which, in turn, means a shorter battery life. Also, if there is a mistake in the Destination Address, the information packet sent may be received by a subsystem, i.e. input/output (I/O) interface, that should not receive the information packet.

Thus, the ability to be able to remotely wake-up a device in the low power mode and to transmit and process information quickly and accurately which is

transmitted through a LAN is of importance to both manufacturers and consumers alike.

SUMMARY OF THE INVENTION

The present invention solves the aforementioned and related problems of remotely waking up a device in a low power mode connected to a node of a network and further transmitting information sent via a LAN to the correct node or device. The present invention discloses a special information packet structure and I/O device used for listening for the special information packet. Once the special information packet is received, the CPU will be activated and the data sent for further processing, if any. If the information packet received by the I/O device is not to be sent to the particular node that is listening for the information, the data will not be sent to that particular node.

An object of the present invention is to be able to remotely wake-up a device coupled to a local area network when there is information to be processed by that particular device in the low power mode.

Another object of the present invention is to be able to transmit information to various users along the network without the use of the central processing unit.

An advantage of the present invention is that the same input/output device present in a standard personal computer can be used.

Another advantage of the present invention is that it can be implemented with very few parts.

Still a further advantage of the present invention is that it uses the same packet structure present in prior systems.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, advantages and features of the present invention will become apparent from the following description, taken in conjunction with the accompanying drawings, in which:

Figure 1 is a block diagram of a personal computer system with low power operation capability that is connected to a network for remote wake-up.

Figure 2 is a schematic view of the remove wake-up packet format of the present invention.

Figure 3 is a block diagram of the remote wake-up section of the network controller of the present invention.

Figure 4 is a block diagram of the wake-up control logic of the network controller of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A description of the information packet and the hardware which functions to generate a signal to wake-up a device in sleep mode via a local area network, will now be described with reference to Figs 1 - 4. Figure 1 shows a block diagram of a digital device having remove wake-up capability. The device, in the most preferred embodiment, is described as a personal computer system connected to one node of a local area network (LAN) having a plurality of nodes with devices coupled thereto. The components that make up the remote wake-up section of the Network Controller as set out in greater detail in Figs. 3 and 4 below, are placed on a single integrated circuit (IC) chip. However, other levels of integration are possible. For example, the Network Controller and the Power Management Logic may be placed on an IC chip. Also, all of the components that make up the device may be placed on a single IC chip or a series of chips. Further, it will be known to those of ordinary skill in the art that the personal computer system represented here can be a more complex system.

In the preferred embodiment, the personal computer system 10 is connected to one node of the computer network, which in this case is the ethernet, via line 11. The ethernet is coupled to the network

controller 12, which in turn is coupled to the Central Processing Unit (CPU) 14, Memory Unit 16, and Disk 18 of the personal computer system 10 via the system data bus. The network controller 12, which is located within the input/output (I/O) subsystem of the personal computer system 10 is also coupled to a Power Management Logic Block 20 via wake-up line 13 and an active low sleep line ~~(SLEEP)~~ 15. The Power Management Logic Block 20 is coupled to the CPU 14 for providing power conservation capability to the personal computer system 10. The powering down of the components of a personal computer system 10 is known to those of ordinary skill in the art and will not be discussed further herein.

The structure of the information packet 50 which is transmitted through the ethernet and contains the remote wake-up information of the present invention is shown in Figure 2. The information packet 50 that is transmitted through the ethernet is generated by a source node remote from the personal computer system 10 by a combination of software and hardware similar to that discussed above. It is understood that any node coupled to a network can act as a source node for transmitting information to the other nodes of the network. The personal computer system 10 of the present invention in conjunction with the appropriate

software and hardware (not shown) can act as a source node and transmit information to the plurality of nodes coupled to the network. The information packet 50 is partitioned into 6 different fields. The first field contains the 6-byte Destination Address 52 indicating where the information packet 50 is to be sent. The second field contains a 6-byte Source Address 54 indicating where the information packet 50 originated from. The third field is a 2-byte length field 56 which contains the length of the frame data within the information packet 50. The fourth field is the Frame Data block 58 which may vary from 0 to 1404 bytes in length containing the data to be processed. In the preferred embodiment of the present invention a 96 byte wake-up data sequence 60, comprising 16 consecutive repetitions of the Destination Address 52 is embedded within the Frame Data block 58. The wake-up data sequence can be located anywhere within the Frame Data block 58. Finally, the sixth field contains a 4-byte Cyclic Redundancy Check (CRC) error control code 62 for checking the accuracy and reliability of the data 58 that was transferred by the information block 50. The total length of the information packet 50 of the present invention may vary from 114 to 1518 bytes. The functions of the

particular information packet 50 discussed above will be described in greater detail below.

Figure 3 illustrates in greater detail, the components which comprise the remote wake-up section of the network controller 12 of the present invention. Data from the information packet 50 transmitted through the ethernet 11 is sent to a comparator 104 via line 11. The comparator 104 is also coupled to a 48 bit Physical Address RAM 106 that is separated into six (6) 8-bit registers, containing the address of the personal computer system 10, via line 105. The output of the comparator 104 is transmitted to the wake-up control logic block 102 via compare okay line 103. The other inputs to the wake-up control logic block 102 are the wake-up enable line 13 which is transmitted from inside the network controller 12, a byte clock signal on line CLK and the carry 2 output line from the binary counter 110 via line 113. The wake-up control logic 102 is further coupled to the RESET pin of the binary counter 110 and a modulo 6 counter 108 via line 109. Three outputs of the modulo 6 counter 108 are transmitted to the Physical Address RAM 106 via line 107. The other output of the modulo 6 counter, the carry 1 output, is transmitted to the binary counter 110 via line 111. The function of the

network controller 12 will be described in greater detail below.

Figure 4 illustrates a schematic diagram of the wake-up control logic 102 of the present invention. The carry 2 output line of the binary counter 110 is transmitted to the SET pin of the D flip flop ("flip flop") 200 via line 113. The byte clock CLK signal is transmitted to the clock input of the flip flop 200. The wake-up enable line 13 is transmitted to both the active low RESET pin 201 of the flip flop 200 and to one input to NAND gate 202. The second input to the NAND gate 202 is the compare okay line from the comparator 104 on line 103. The output of the NAND gate 202 is fed into both the RESET pin of the modulo 6 counter 108 and the RESET pin of the binary counter 110 via line 109. The output of the flip flop 200 is fed back into its input via line 203 and further acts as the wake-up frame received output line 101 of the system. The function of the wake-up logic 102 will be discussed in greater detail below.

The operation of the wake-up control logic 102 to generate the signal which powers up the personal computer system 10 of the present invention will now in be described with reference to Figs. 3 and 4. The personal computer system 10 must be in a low power (sleep) mode before any wake-up capability is

available. Thus, the Power Management Logic Unit 20 puts the personal computer system 10 into the low power mode by asserting the SLEEP line 15 to an active low (0V) state. When the SLEEP line 15 is active low, the wake-up enable line 13 is made active high, thereby placing the network controller 12 into the remote wake-up mode. When the network controller 12 is in the remote wake-up mode, it listens to the ethernet via line 11 for any information packets 50 that are being transmitted through the ethernet via line 11. When an information packet 50 reaches the personal computer system 10, it is first transmitted to the comparator 104 via line 11 where the Destination Address 52 of the information packet 50 is compared to the output of the Physical Address RAM 106 which has been loaded with the node address of the personal computer system 10 on line 105 to determine if the particular Destination Address 52 is connected to the node serviced by the particular network controller 12. If there is an address match, the compare okay line 103 is asserted active high and transmitted to the wake-up control logic block 102 via line 103. As long as there is an address match, the compare okay line 103 will remain active high. The wake-up enable line 13 is asserted via the SLEEP line 15. The wake-up enable line 13 is also used as a

remote wake-up acknowledgement when the SLEEP line 15 is deasserted. After the comparator 104 receives the Destination Address 52 contained within the information packet 50, the Frame Data field 58 of the packet 50 is read to determine if the Destination Address 52 is present at least 16 consecutive times within the frame data 58 of the information packet 50. For each consecutive byte of received data, the byte clock line is toggled via line CLK incrementing the counters of both the modulo 6 counter 108 and the binary counter 110. When the modulo 6 counter 106 counts six transitions of the byte clock on line CLK the carry 1 output becomes active high and is transmitted to the binary counter 110 via line 111. The binary counter 110 continues to increment on each transition of the byte clock on line CLK until it reaches 16. At this point, the carry 2 line 113 becomes active high and is transmitted to the SET pin of the flip flop 200 of the wake-up control logic 102. When the count of the binary counter 110 reaches 16, this signifies that the frame data 58 of the information packet 50 needs to be processed by the CPU 14 of the personal computer system 10. The asserted carry 2 line 113 that is transmitted to the SET pin of the flip-flop 200, results in a wake-up signal on line

101 that is transmitted to the Power Management Logic 20 which indicates that the CPU 14 should be activated. After the Power Management Logic 20 has acknowledged the wake-up signal on line 101, the SLEEP line 15 is deasserted which deasserts the wake-up enable line 13. The compare okay line 103 is also made active low, thereby causing the output of the NAND gate 202 on line 109 to become active high thus resetting the modulo 6 counter 108 and the binary counter 110 to zero.

Once the frame data 58 has been transmitted from the network controller 12 to the CPU 14 of the personal computer system 10, the personal computer system 10 will stay in the active state while there is processing being done on the frame data 58 that is read from future information packets 50 received by the network controller 12. Once the processing of the frame data 58 is complete, and after a predetermined time of inactivity, the Power Management Logic 20 will again power down the personal computer system 10 by making the SLEEP line 15 active low which will assert the wake-up line 13, thereby putting the personal computer system 10 back in the remote wake-up mode to listen for another information packet 50.

The foregoing description of the preferred embodiment of the present invention has been presented

for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teaching. The system and method described for the remote wake-up of a personal computer system was chosen and described in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. For example, the personal computer system may be placed in the sleep mode via software control. It is intended that the scope of the invention be defined by the claims appended hereto.

CLAIMS

What is claimed is:

1. A system for remotely waking a device coupled to a communication link, comprising:

means for processing information;

means for transmitting information coupled to said processing means;

means for controlling the transfer of information between said processing means and said transmitting means, said controlling means including means for activating said processing means; and

power conservation means for powering down said processing means.

2. The system of Claim 1, wherein said controlling means further comprises:

means for receiving information from a network; and

circuitry operative to generate a remote activation signal to transmit to said processing means.

3. A system for remotely waking a device coupled to a communication link, comprising:

a microprocessor;

a memory coupled to said microprocessor which stores information;

a power circuit operatively connected to power down said processor; and

a controller coupled to a network, said controller operative to generate a control signal to remotely power up said microprocessor.

4. The system of Claim 3, wherein said controller comprises a counter.

5. The system of Claim 3, wherein said controller comprises circuitry operative to generate a power up signal.

6. A method for remotely waking a device coupled to a communication link which comprises the steps of:

(a) receiving a power down signal from power conservation circuitry;

(b) receiving an information packet over a network;

(c) determining whether said information packet should be transmitted to a device coupled to said network;

(d) generating a control signal operative to activate said device; and

(e) transmitting said information packet to said device.

7. The method of Claim 6 wherein step (c) comprises the steps of:

(f) reading the destination address of said information packet;

(g) determining whether said destination address occurs at least a variable N consecutive times in the data field of said information packet, where N is an integer greater than 1.

8. The method of Claim 7 wherein step (g) comprises the step of:

(h) incrementing a counter for each consecutive occurrence of said destination address in said data field of said information packet.

9. The method of Claim 7, wherein said variable N equals 16.

10. A method for remotely waking a device coupled to a communication link which comprises the steps of:

(a) receiving an information packet from a network;

(b) reading the destination address from said information packet;

(c) determining whether said destination address occurs sixteen (16) consecutive times in the data field of said information packet;

(d) generating a control signal to power up a device after sixteen (16) consecutive occurrences of said destination address in said data field of said information packet; and

(e) transmitting said information packet.

11. A circuit for generating a wake-up signal, comprising:

means for sending information;

means for receiving information;

means for processing information;

means for transmitting information coupled to said processing means;

means for controlling the transfer of information between said processing means and said transmitting means, said controlling means including means for generating a power up signal.

12. The circuit of Claim 11, wherein said controlling means comprises:

means for receiving information transmitted from said source means; and

circuitry operative to generate a signal to power up said processing means.

13. An integrated circuit for generating a wake-up signal, comprising:

circuitry operative to power down a microprocessor; and

a controller coupled to a network, said controller operative to generate a signal to power up said device.

14. The integrated circuit of Claim 13, wherein said controller comprises a counter.

15. The integrated circuit of Claim 13, wherein said controller comprises circuitry operative to generate a power up signal.

16. The integrated circuit of Claim 13, wherein said controller comprises means for reading information transmitted through said network.

17. A network controller integrated circuit chip, comprising:

means for receiving information from a network; and

means for generating a wake-up signal to power up a device.

18. The network of Claim 17, wherein said generating means comprises a plurality of counters.

19. The network controller chip of Claim 17, wherein said generating means comprises circuitry responsive to a signal from said plurality of counters which generates a power up signal.

20. A system, comprising:

a plurality of nodes coupled to a network;

a device coupled to one of said plurality of nodes, said device having means within said device for receiving information from said network; and

a controller coupled to said receiving means, said controller including circuitry responsive to said information from said network which generates a wake-up signal.

21. The system of Claim 20, wherein said circuitry comprises a counter and circuitry responsive to a signal from said counter which generates a power up signal.

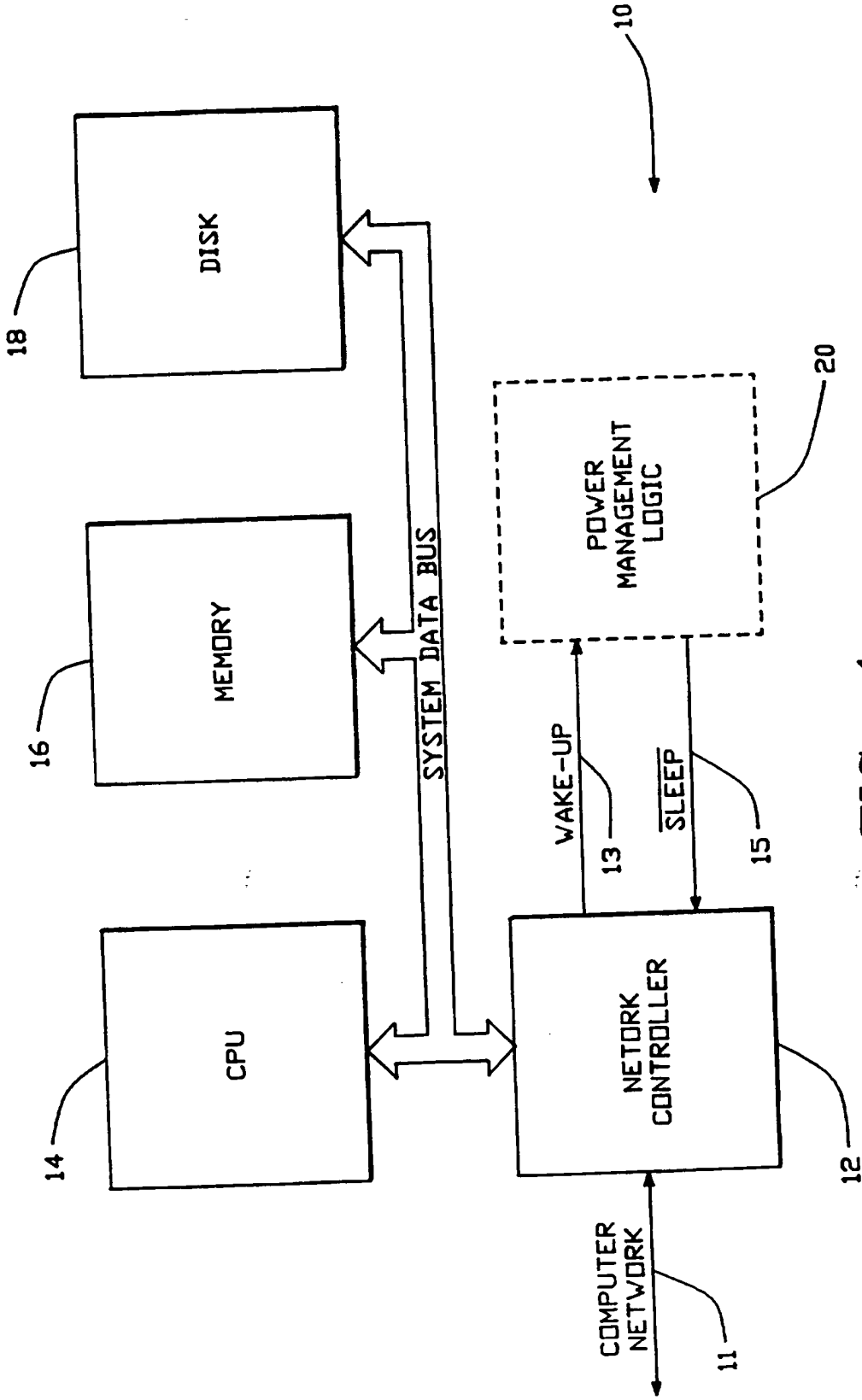
10
DISK
18
MEMORY
16
CPU
14
SYSTEM DATA BUS
POWER MANAGEMENT LOGIC
20
WAKE-UP
13
SLEEP
15
NETORK CONTROLLER
12
COMPUTER NETWORK
11

FIG.—1

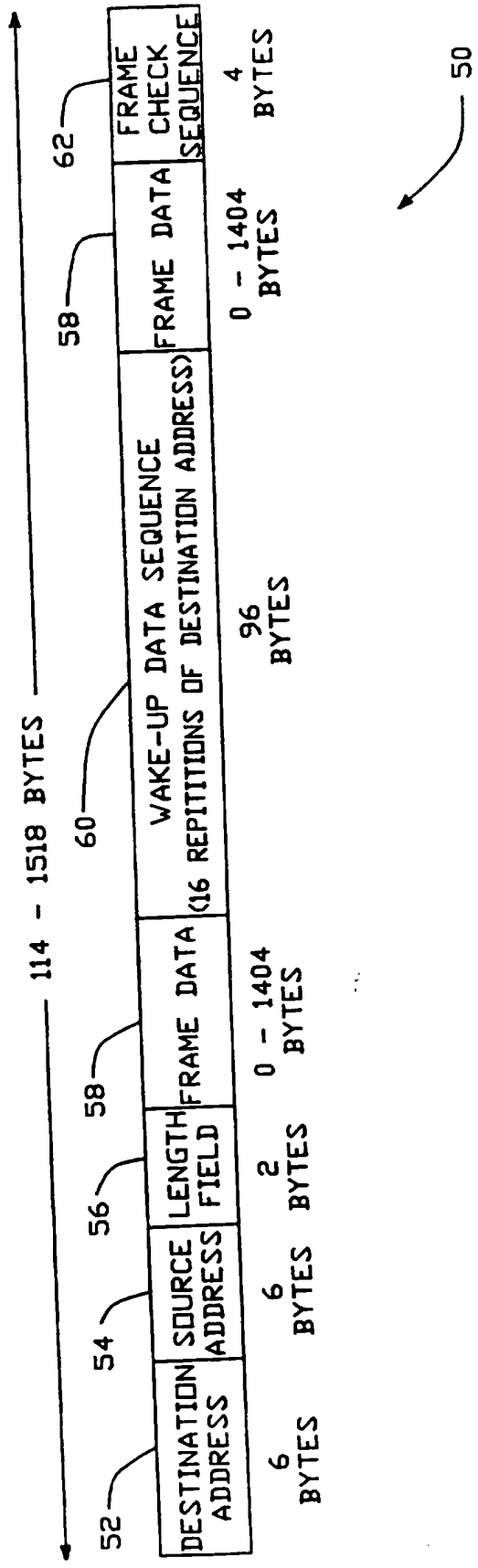
114 - 1518 BYTES
DESTINATION ADDRESS
SOURCE ADDRESS
LENGTH FIELD
FRAME DATA
WAKE-UP DATA SEQUENCE (16 REPITITIONS OF DESTINATION ADDRESS)
FRAME DATA
FRAME CHECK SEQUENCE
52
54
56
58
60
58
62
6 BYTES
6 BYTES
2 BYTES
0 - 1404 BYTES
96 BYTES
0 - 1404 BYTES
4 BYTES
50

FIG.-2

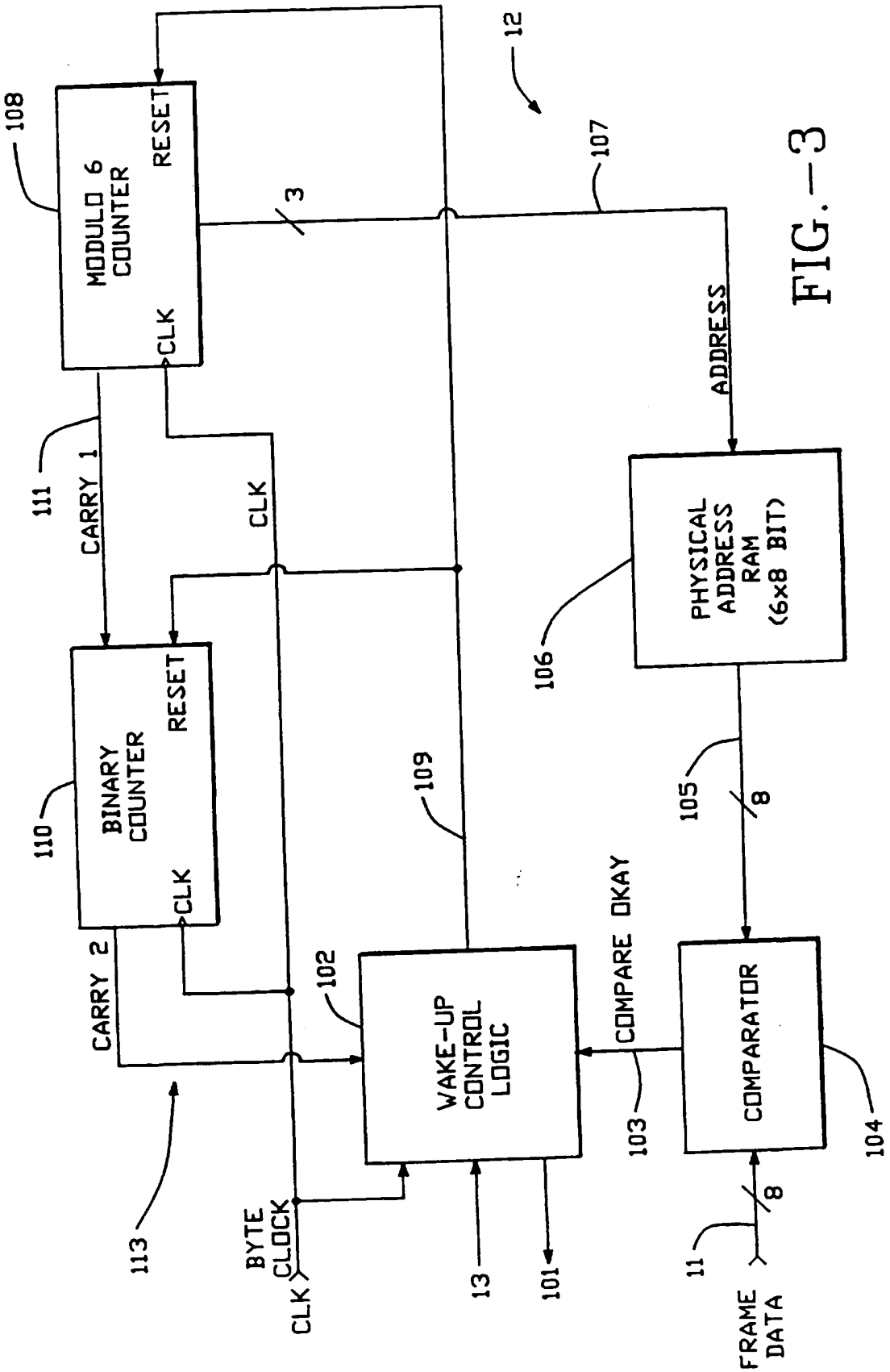
12
108
MODULO 6 COUNTER
RESET
CLK
3
107
ADDRESS
111
CARRY 1
CLK
PHYSICAL ADDRESS RAM (6x8 BIT)
106
BINARY COUNTER
RESET
110
CLK
109
105
8
CARRY 2
102
WAKE-UP CONTROL LOGIC
COMPARE OKAY
COMPARATOR
103
104
113
BYTE CLOCK
CLK
13
101
11
8
FRAME DATA

FIG.—3

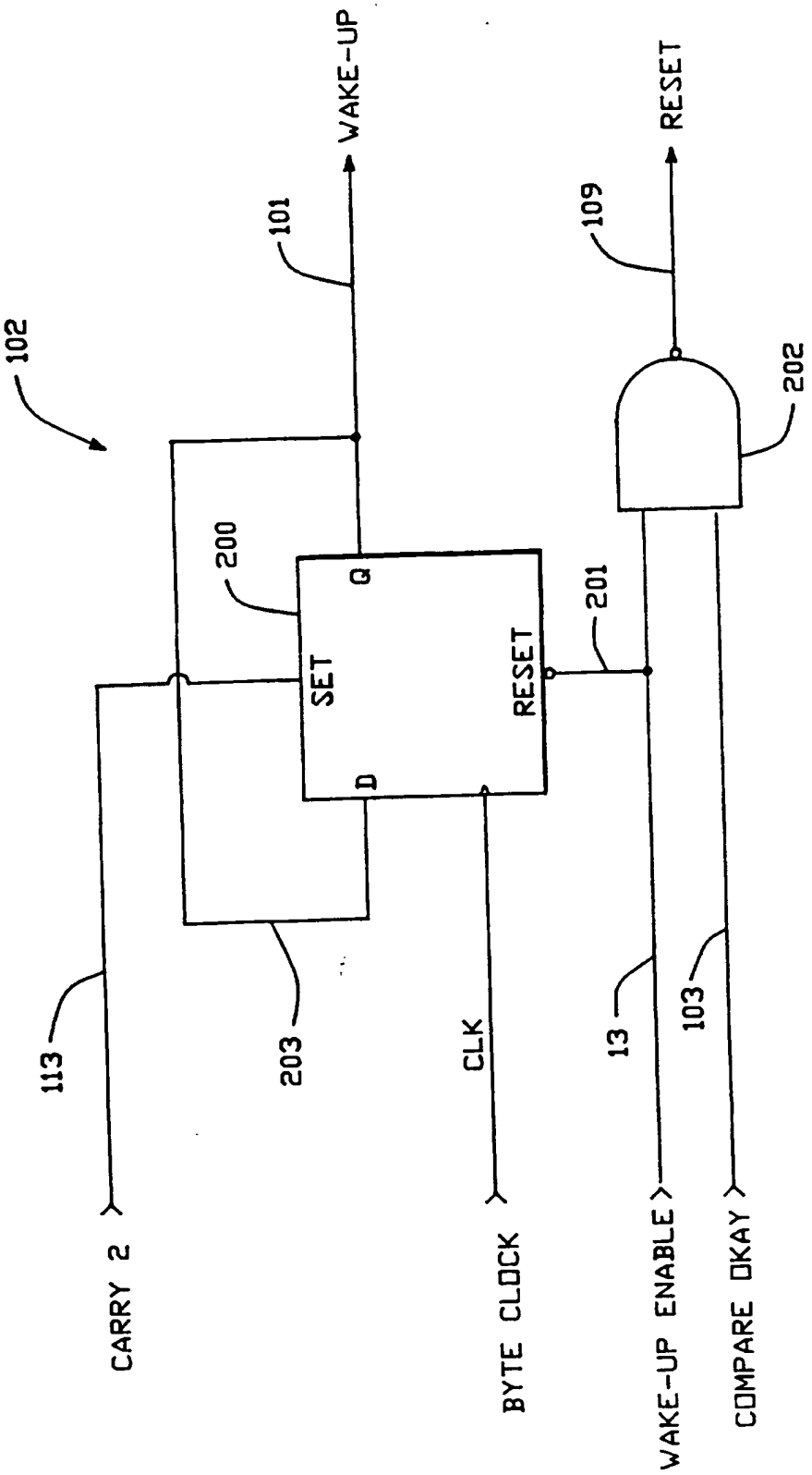
WAKE-UP
RESET
101
109
102
202
200
Q
SET
RESET
201
D
113
203
CLK
13
103
CARRY 2
BYTE CLOCK
WAKE-UP ENABLE
COMPARE OKAY

FIG.—4

INTERNATIONAL SEARCH REPORT

Ir nal Application No
PCT/US 95/12128

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L12/12 G06F1/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP-A-0 573 204 (ADVANCED MICRO DEVICES, INC) 8 December 1993 see page 2, line 32 - line 54 see page 3, line 37 - page 4, line 27	1-3,5,6, 11-13, 15-17,20
Y		4,14,21
A		7-10

X	US-A-5 012 233 (POULSEN JR) 30 April 1991 see column 2, line 25 - column 4, line 9 see column 5, line 24 - line 31	1,2,11, 12
Y		4,14,21
A		3,6, 8-10, 17-20

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
21 December 1995	05.01.96

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 95/12128

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US-A-4 181 909 (PYEATTE ET AL.) 1 January 1980 see column 2, line 17 - line 50 see column 4, line 40 - line 60 -----	1,2,4, 6-10,14, 18,19,21

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
PCT/US 95/12128

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		JP-A-	6037765	10-02-94
US-A-5012233	30-04-91	NONE		
US-A-4181909	01-01-80	DE-A-	2903646	09-08-79